## LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An amplifier architecture comprising:

a switching amplifier operative to amplify an input signal;

a supply control device that varies a supply voltage of the switching amplifier between a plurality of fixed voltage supply levels based on a characteristic of the input signal relative to a threshold level; and

a binary waveform converter that converts the input signal into a binary waveform for inputting into the switching amplifier.

2. (Original) The amplifier architecture of claim 1, further comprising a digital-to-analog converter (DAC) that converts the binary waveform into an analog waveform for amplifying by the switching amplifier.

3. (Original) The amplifier architecture of claim 2, the DAC comprising a one-bit DAC.

4. (Original) The amplifier architecture of claim 1, the input signal being an n-bit word that represents a phase and/or amplitude modulated signal and the threshold level being an envelope amplitude level associated with the input signal representation.

5. (Original) The amplifier architecture of claim 4, the switching amplifier being a peak amplifier configured in combination with a main amplifier, the peak amplifier receiving the binary waveform for input signals above the threshold and the peak amplifier effectively being turned "OFF" for input signals below the threshold.

6. (Original) The amplifier architecture of claim 5, the main amplifier receiving the binary waveform for both peak and average level signals.

7. (Original) The amplifier architecture of claim 5, the main amplifier effectively being turned "OFF" for input signal levels above the threshold by one of providing a zero like signal to the input of the main amplifier and setting the supply level to a very low level effectively turning it "OFF" for input signal levels above the threshold.

8. (Original) The amplifier architecture of claim 5, the peak amplifier effectively being turned "OFF" for input signal levels below the threshold by one of providing a zero like signal to the input of the peak amplifier and setting the supply level to a very low level effectively turning it "OFF" for input signal levels below the threshold.

9. (Currently Amended) The amplifier architecture of claim 1, further comprising a digital control device that analyzes the input signal and builds a fixed voltage supply level adjustment profile for dynamically modifying the supply voltage to the switching amplifier in response to changes in the characteristic of the input signal relative to the threshold level.

10. (Original) The amplifier architecture of claim 1, the binary waveform converter comprising a delta sigma modulator.

11. (Original) The amplifier architecture of claim 1, further comprising a digital control device that generates a reference signal corresponding to a desired output signal of the switching amplifier, the clean reference signal being combined with a portion of an output signal from the switching amplifier to determine an error signal, the error signal being inverted and combined with a delayed version of the output signal of the switching amplifier to generate a final output signal.

12. (Original) The amplifier architecture of claim 1, the supply control device comprising a DC/DC converter.

13. (Original) A transmitter comprising the amplifier architecture of claim 1.

14. (Original) A base station comprising the transmitter of claim 13.

15. (Currently Amended) A system for amplifying a signal comprising:

a binary waveform converter that converts an n-bit word representing an input signal into a binary waveform;

a digital-to-analog converter (DAC) that converts the binary waveform into an analog binary waveform;

a switching amplifier ~~that amplifies~~ operative to amplify the analog binary waveform; ~~and~~

a main amplifier operative to amplify the analog binary waveform, the main amplifier and the switching amplifier being configured such that the switching amplifier operates as a peak amplifier; and

a digital control device that modifies a configuration of the system in response to changes in at least one characteristic associated with the input signal.

16. (Original) The system of claim 15, the modification of the configuration comprising adjusting the supply and/or bias of the switching amplifier.

17. (Canceled)

18. (Currently Amended) The system of claim ~~17~~ 15, the main amplifier comprising a linear amplifier.

19. (Currently Amended) The system of claim ~~17~~15, the modification of the configuration comprising switching the analog binary waveform to the input of the switching amplifier for peak level signals and providing a zero-like signal to the input of the switching amplifier for average level signals.

20. (Currently Amended) The system of claim ~~17~~ 15, the switching amplifier effectively being turned "OFF" for average level signals by setting the supply level to a ~~very~~ low level effectively turning it "OFF" for average level signals.

21. (Currently Amended) The system of claim ~~17~~ 15, the main amplifier effectively being turned "OFF" for peak level signals by one of providing a zero like signal to the input of the main amplifier and setting the supply level to a ~~very~~ low level effectively turning it "OFF" for peak level signals.

22. (Original) The system of claim 15, the DAC comprising a one-bit DAC and the binary waveform converter comprising a delta sigma modulator.

23. (Original) The system of claim 15, the input signal being a representation of a phase and/or amplitude modulated signal and the characteristic being an envelope amplitude level associated with the input signal representation.

24. (Original) The system of claim 15, the digital control device analyzes the input signal and builds a voltage supply level profile for dynamically adjusting the supply and/or bias of the switching amplifier in response to changes in the at least one characteristic associated with the input signal.

25. (Currently Amended) An amplification system comprising:

means for converting an n-bit binary word representing a phase and amplitude modulated input signal into a binary waveform;

means for amplifying the binary waveform to reproduce the phase and amplitude modulated input signal; and

means for modifying the supply and/or bias of the means for amplifying between a plurality of fixed voltage supply levels in response to changes in a characteristic of the input signal.

26. (Currently Amended) The system of claim 25, further comprising means for converting the binary waveform into an analog binary waveform prior to amplification.

27. (Currently Amended) The system of claim 25, further comprising means for building a fixed voltage supply level adjustment profile for dynamically modifying the supply voltage to the switching amplifier in response to changes in the characteristic of the input signal relative to a threshold level.

28. (Original) The system of claim 25, further comprising means for linearizing the output signal of the means for amplifying.

29. (Original) The system of claim 28, the means for linearizing comprising a digital cross-cancellation component that generates a separate reference signal corresponding to a desired output signal, the clean separate signal being combined with a portion of an output signal from the means for amplifying to determine an error signal, the error signal being inverted and combined with a delayed version of the output signal of the means for amplifying to generate a final output signal.

30. (Original) The system of claim 29, further comprising means for reducing peaks associated with the n-bit binary word.

31. (Currently Amended) A method of amplifying an input signal with a switching amplifier, the method comprising:

determining a fixed voltage supply level adjustment profile based on changes in at least one characteristic associated with an input signal;

converting a digital input signal into a single bit binary waveform;

converting the single bit binary waveform into an analog binary waveform; and

amplifying the analog binary waveform with a switching amplifier into an amplified output signal while concurrently adjusting a supply and/or bias level of the switching amplifier between a plurality of fixed voltage supply levels based on the fixed voltage supply level adjustment profile.

32. (Original) The method of claim 31, further comprising transmitting the amplified input signal to at least one receiver.

33. (Original) The method of claim 31, the converting a digital input signal into a single bit binary waveform comprising delta sigma modulating the digital input signal.

34. (New) The amplifier architecture of claim 1, the switching amplifier comprising at least one of inhibiting electronics, harmonic termination and zoning filers that facilitate the reproduction of a desired amplified output signal within a desired spectrum.